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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/808,059 | 03/24/2004 | Leonard Forbes | 400.285US01 | 4221 |

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| EXAMINER | |
|---|---|
| PIZARRO CRESPO, MARCOS D | |
| **ART UNIT** | **PAPER NUMBER** |
| 2814 | |

DATE MAILED: 11/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/808,059 | FORBES, LEONARD | |
| | Examiner | Art Unit | |
| | Marcos D. Pizarro-Crespo | 2814 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *10/19/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1,2,4,6 and 49-55* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,6 and 49-55* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1,2,4,6 and 49-55* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Attorney's Docket Number: 400.285US01
Filing Date: 3/24/2004
Claimed Foreign Priority Date: none
Applicant(s): Forbes
Examiner: Marcos D. Pizarro-Crespo

## DETAILED ACTION

This Office action responds to the amendment filed on 10/19/2006.

### *Continued Examination Under 37 CFR 1.114*

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after the final rejection mailed on 4/6/2006. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/19/2006 has been entered.

### *Acknowledgment*

2. The amendment filed on 10/19/2006, responding to the Office action mailed on 4/6/2006, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this Office action are claims 1, 2, 4, 6, and 49-55.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

**4. Claims 1, 2, 6, and 49-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugizaki in view of Yu (US 6495437).**

5. Regarding claim 1, Sugizaki shows (see, *e.g.*, fig. 1) most aspects of the instant invention including an NROM memory transistor comprising:

- ✓ A substrate
- ✓ A plurality of source/drain regions with a different conductivity than the substrate
- ✓ A nanolaminate, high-permittivity (high-k), metal-oxide gate-dielectric composed of oxide–aluminum oxide–oxide and overlying the substrate
- ✓ A control gate formed on top of the gate dielectric

6. Regarding claims 1, 2, and 6, it is noted that Sugizaki shows most aspects of the semiconductor device according to the claimed invention (see, *e.g.*, paragraphs 5 above), except for the aluminum oxide being an *oxidized* aluminum oxide having a first concentration of excess aluminum at a first oxide interface adjacent the substrate, a second concentration of excess aluminum at a second oxide interface adjacent the control gate, and a method of forming oxidized aluminum oxide by the low-temperature oxidation of aluminum, wherein the first concentration of excess aluminum is greater than the second concentration of excess aluminum, and wherein the oxidized aluminum has a larger energy barrier at the second oxide interface than at the first oxide interface.

7. Yu (see, *e.g.*, col.7/ll.23-33), on the other hand, teaches using a low-temperature oxidation step to form the aluminum oxide of Sugizaki as an oxidized aluminum gate dielectric. Yu teaches that doing so would result in a substantial uniform thickness for the gate dielectric and that although other processes may be used such are not preferred as they may result in undesirable non-uniform thicknesses for the gate dielectric (see, *e.g.*, col.7/ll.33-38).

8. Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art to form Sugizaki's aluminum oxide by the low temperature oxidation of a metal, as suggested by Yu, because doing so would result in a gate dielectric having a substantial uniform thickness.

9. Although Sugizaki/Yu fail to specify that there is a first concentration of excess aluminum at the first oxide interface adjacent to the substrate, and a second concentration of excess aluminum at the second oxide interface adjacent the control gate, wherein the first concentration is greater than the second concentration, they do show that the aluminum oxide layer is formed by the low-temperature oxidation of Al (see, *e.g.*, Yu/col.7/ll.23-38). As recognized by the applicant (see, *e.g.*, pp.3 of the amendment filed on 7/6/2006), it is taught by the present specification (see, *e.g.*, par.0046-0047) that forming the gate dielectric by the low temperature oxidation of aluminum would result in an $Al_2O_3$ layer having a much more stoichiometric composition at the interface with the top oxide layer than at the interface with the tunnel oxide layer. In other words, forming $Al_2O_3$ by the low-temperature oxidation of Al will result in the concentration of Al ions being lower at the interface with the top oxide than at the

interface with the bottom oxide. Because of this concentration gradient, the tunnel barrier will be higher at the top oxide than at the bottom oxide (see, *e.g.*, par.0046). The applicant also included in his remarks on page 3 of the amendment that one skilled in the art would recognize that the above only applies to the claimed oxidized aluminum structure.

10. In view of the above, the claimed aluminum concentrations and energy barriers recited in claims 1 and 6 are necessarily present in Sugizaki/Yu, and persons of ordinary skill would so recognize it.

11. Regarding claim 49, Yu shows the source/drain regions are n+ type doped silicon (see, *e.g.*, col.4/ll.15).

12. Regarding claim 50, Yu shows the control gate is a polysilicon material (see, *e.g.*, col.4/ll.65).

13. Regarding claim 51, Yu shows the substrate is a p+ type silicon material (see, *e.g.*, col.4/ll.10).

**14. Claims 4 and 52-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sugizaki/Yu in view of Akatsu (US 5717635).**

15. Regarding claim 4, Sugizaki/Yu shows most aspects of the instant invention (see, *e.g.*, paragraphs 5-10 above). They, however, fail to show that the transistor is in either a NOR-type flash memory structure of a NAND-type flash memory structure. Sugizaki, however, teaches that the transistor is a flash memory device (see, *e.g.*, abstract). At the present time, there are two basic architectures for memory cell arrays referred to as NOR-type and NAND-type respectively (see, *e.g.*, Akatsu/col.4/ll.50-57). The NAND-

type, however, lends itself to much higher integration densities (see, *e.g.*, Akatsu/col.5/ll.34-40).

It would have been obvious at the time of the invention to one of ordinary skill in the art to have Sugizaki/Yu's transistor in a NAND-type memory structure, as suggested by Akatsu, to achieve high-integration density.

16. Regarding claim 52, Sugizaki shows (see, *e.g.*, fig. 1) most aspects of the instant invention including an NROM memory transistor comprising:

- ✓ A substrate having a plurality of source/drain regions having a different conductivity type than the remainder of the substrate
- ✓ A nanolaminate, high permittivity (high-k), metal gate dielectric overlying the substrate and composed of oxide-aluminum oxide-oxide
- ✓ A control gate formed on top of the gate dielectric

17. Regarding claims 52, 53, and 55, see the comments above in paragraphs 6-10 with respect to claims 1, 2, and 6, which are considered repeated here. In addition, although Sugizaki/Yu fail to show the memory transistors being part of a memory array that is coupled to a processor, it is well known that basic computer functions must be supported by arrays of storage devices like Sugizaki/Yu's memory transistors from which data and instructions may be fetched when needed by the computer processor (see, *e.g.*, Akatsu/col.1/ll.12-20). Using Sugizaki' memory transistor in a memory array supporting a processor would provide the array with superior retention characteristics and scarcely any leakage current (see, *e.g.*, Sugizaki/pp.27/col.1/abstract).

18. It would have been obvious at the time of the invention to incorporate Sugizaki/Yu's memory transistor in a memory array, as taught by Akatsu, to support and provide superior retention characteristics to a computer processor.

19. Regarding claim 54, see the comments above in paragraph 15 with respect to claims 4, which are considered repeated here.

### *Response to Arguments*

20. The applicant argues:

> Claim 1 recites, "wherein the oxidized aluminum has a first concentration of excess aluminum at a first oxide interface adjacent the substrate and a second concentration of excess aluminum at a second interface adjacent the control gate" and "wherein the first concentration of excess aluminum is greater than the second concentration of excess aluminum". The cited references, fails to teach or suggest these limitations as both are silent with respect to varying composition of their oxidized aluminum. This is a structural limitation requiring the oxidized aluminum to contain a higher concentration of excess aluminum nearer the substrate and a reduced concentration of excess aluminum nearer the control gate.

The examiner responds:

Although Sugizaki/Yu fail to specify that there is a first concentration of excess aluminum at the first oxide interface adjacent to the substrate, and a second concentration of excess aluminum at the second oxide interface adjacent the control gate, wherein the first concentration is greater than the second concentration, they do show that the aluminum oxide layer is formed by the low-temperature oxidation of Al (see, *e.g.*, col.7/ll.23-38). As recognized by the applicant (see, *e.g.*, pp.3 of the amendment filed on 7/6/2006), it is taught by the present specification (see, *e.g.*, par.0046-0047) that forming the gate dielectric by the low temperature oxidation of aluminum would result in an $Al_2O_3$ layer having a much more stoichiometric composition at the interface with the top oxide layer than at the interface with the tunnel oxide layer.

In other words, the concentration of Al ions would be lower at the interface with the top oxide than at the interface with the bottom oxide. The applicant also included in his remarks on page 3 of the amendment that one skilled in the art would recognize that the above only applies to the claimed oxidized aluminum structure.

21. In view of the above, the claimed aluminum concentrations are necessarily present in Sugizaki/Yu, and persons of ordinary skill would so recognize it.

***Conclusion***

22. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(571) 273-8300**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:00 AM to 7:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

24. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or

Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

25. The following list is the Examiner's field of search for the present Office Action:

| Field of Search | Date |
|---|---|
| U.S. Class / Subclass(es): 257/314,324-326,410,411 | 10/31/2006 |
| Other Documentation: | |
| Electronic Database(s): EAST (USPAT, EPO, JPO) | 10/31/2006 |

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MDP/mdp
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